UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,847	12/02/2003	Keith A. Jenkins	YOR920030553US1(8728-666)	3238

7590 01/21/2005

Frank Chau
F. CHAU & ASSOCIATES, LLP
Suite 501
1900 Hempstead Turnpike
East Meadow, NY 11554

EXAMINER	
NGUYEN, LINH M	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 01/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/725,847	JENKINS ET AL.	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,9-16 and 21* is/are rejected.

7)☒ Claim(s) *4-8 and 17-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-21 are presented in the instant application according to the Applicants' filing on 12/02/2003.

Inventorship

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim Objections/Minor Informalities

2. Claim 17 is objected to because of the following informalities:

Claim 17, line 6, for consistency of the claim language, it is suggested to change "binary" to -- random--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1-3, 9-16 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Miethig et al. (U.S. Patent No. 6,593,871).

With respect to claim 1, Miethig et al. discloses, in Figures 2-4, a programmable jitter signal generator comprising a) a jitter distribution control unit [Fig. 1, items 240,250,244,234; Fig.4, item 22]; b) a selection unit [222] in signal communication with the jitter distribution control unit; and c) a delay unit [212] in signal communication with the selection unit.

With respect to claim 2, Miethig et al. discloses, in Figures 2 and 3, that the delay unit comprises a delay chain [212].

With respect to claim 3, Miethig et al. discloses, in Figures 2 and 3, the selection unit comprises a multiplexer [222].

With respect to claim 9, Miethig et al. discloses, in Figures 2 and 3, that the delay unit [212] comprising a modified delay chain having at least one inverter [212A] coupled to the output of a delay chain [212].

With respect to claim 10, Miethig et al. discloses, in Figures 2 and 3, that the delay unit comprising a modified delay chain having at least one logical gate [212A *(inverters are logical gates)*] coupled to the input of a delay chain [212].

With respect to claim 11, Miethig et al. discloses, in Figures 2-4, a method of generating a programmable jitter signal, the method comprising a) programming a control unit [Fig. 1, items

240,250,244,234; Fig. 4, item 22]; b) receiving a reference signal [Fig. 2, CLOCK], c) delaying [Fig. 2, 212] the received reference signal by a multiple of a base time increment, and d) selecting [222] a delayed reference signal delayed by a desired multiple of the base time increment in accordance with the programmed control unit.

With respect to claim 12, Miethig et al. discloses, in Figures 2-4, that each multiple of the base time increment corresponds to one of a plurality of delay cells [Fig. 3, item 212A], and the delayed reference signal [Fig. 2, item 224] is selected by selecting a delay cell corresponding to the programmed delay of the output.

With respect to claim 13, Miethig et al. discloses, in Figures 2-4, that delaying the reference signal comprises adjusting the time instants of the rising edge of the received reference signal [Fig. 1, CLOCK].

With respect to claim 14, Miethig et al. further discloses, in Figures 2-4, controlling the jitter distribution of an output signal in accordance with the programmed control unit [Fig. 1, items 240,250,244,234; Fig. 4, item 22].

With respect to claim 15, Miethig et al. further discloses, in Figures 2-4, controlling the average jitter magnitude of an output signal in accordance with the programmed control unit [Fig. 1, items 240,250,244,234; Fig. 4, item 22].

With respect to claim 16, Miethig et al. discloses, in Figures 2-4, that selecting the delayed reference signal comprises multiplexing the delayed reference signal [Fig. 1, item 224] from one of a plurality of delay cells [Fig. 2, item 212A] in accordance with the output of the programmed control unit [Fig. 1, items 240,250,244,234; Fig. 4, item 22].

With respect to claim 21, Miethig et al. further discloses, in Figure 2, inverting [212A] the output of a delay chain.

Allowable Subject Matter

5. Claims 4-8 and 17-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter:

The closest prior art of record does not show or fairly suggest:

a) A programmable jitter signal generator, in which the jitter distribution control unit includes a random access memory in signal communication with a binary counter; and a random number generator in signal communication with the random access memory, as called for in dependent claim 4;

b) A programmable jitter signal generator, in which the jitter distribution control unit includes a plurality of flip-flop devices, at least one summing device having one input coupled to the output of a first flip-flop device, and an output coupled to the input of a second flip-flop device, and at least one gain device having an output coupled to a second input of the at least one flip-flop device, as called for in dependent claim 6;

c) A method, in which programming a control unit includes generating a random number in correspondence with a binary counter and storing the generated random number for later retrieval, as called for in dependent claim 17;

d) A method, in which programming a control unit includes providing a plurality of flip-flop devices, providing at least one summing device having one input coupled to the output of a

first flip-flop device, and an output coupled to the input of a second flip-flop device, providing at least one gain device having an output coupled to a second input of the at least one flip-flop device, and assigning the gain of the at least one gain device, as called for in dependent claim 18.

Citation of Relevant Prior Art

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Prior art Livolsi (U.S. Patent No. 6,404,257) discloses a variable delay element for jitter control in high speed data links.

Prior art Livolsi (U.S. Patent No. 6,384,661) discloses a multi level jitter pre-compensation logic circuit for high speed data links.

Prior art Walker (U.S. Patent No. 6,285,197) discloses a system and method for generating a jittered test signal.

Prior art Arai (U.S. Patent No. 5,103,185) discloses a clock jitter suppressing circuit.

Prior art Uchiyama (JP. Patent No. JP403278376A) discloses a jitter generating method and a symmetry generating method by delay element.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMN

LINH MY NGUYEN
PRIMARY EXAMINER